

Naga B.

Expert Senior Staff Engineer- RTL

SUMMARY

- 12+ years in front-end RTL design for 5G wireless modems, ASIC/FPGA, and high-speed memory interfaces (DDR).
- Expertise in Verilog, VHDL, SystemVerilog, and tools like Xilinx Vivado, Intel Quartus, ModelSim, and Synopsys DC.
- Led RTL design and verification for complex 5G NR projects, including JESD204C/D, ORAN, and PTP IPs.
- Proficient in ASIC front-end flow, timing closure, CDC, and DO-254 design guidelines.
- Strong background in FPGA integration, board testing, and multi-team collaboration across global projects.

TECHNICAL SKILLS

Main Technical Skills	Verilog (5 yr.), VHDL (5 yr.), Unix (5 yr.), Ant Design (5 yr.)
Programming Languages	Tcl (5 yr.), Verilog (5 yr.)
Java Frameworks	Hibernate
Mobile Frameworks and Libraries	OneSignal (5 yr.)
Databases & Management Systems / ORM	Hibernate
UI Frameworks, Libraries, and Browsers	Ant Design (5 yr.), Material UI (5 yr.)
Amazon Web Services	AWS Aurora (5 yr.)
Azure Cloud Services	Azure AD hybrid identity, Azure Logic Apps
Methodologies, Paradigms and Patterns	Architecture and Design Patterns, microservices
Web/App Servers, Middleware	GlassFish (5 yr.)
Hardware	I2C, SPI
Operating Systems	Linux, Unix (5 yr.), Windows
iOS Libraries and Tools	Packet Tunnel Provider
Blockchain and Decentralized Software	Payload Verification (A2SPA)
QA, Test Automation, Security	REST-Assured (5 yr.)

Third Party Tools / IDEs / SDK / Services	Sublime Text
UI/UX/Wireframing	UI/UX
Version Control	VCS (5 yr.)
Other Technical Skills	CDC, Closures (5 yr.), CPRI (5 yr.), CRO, eCPRI (5 yr.), IES (5 yr.), Illustration and icons (5 yr.), JESD204B, JESD204C (5 yr.), JESD204D (5 yr.), LVDS (5 yr.), MAC Algorithm, ModelSim (5 yr.), ORAN (5 yr.), PCIe (5 yr.), PlanAhead, PTP (5 yr.), Quartus (5 yr.), SOC, SRIO (5 yr.), Verdi (5 yr.), XILINX, Xilinx Vivado (5 yr.), Zynq Ultrascale+ (5 yr.)

WORK EXPERIENCE

Senior FPGA Consultant - Confidential, UAE (Satcom HT NB 75KHz B.W Waveform Design and Verification)

Duration: May 2025 - Present

Summary: Project focused on the design and verification of satellite communication waveform with 75KHz bandwidth, involving TX and RX chain integration on Xilinx Ultrascale FPGA.

Responsibilities:

- RTL design for TX chain and RX modules including Peak Detector and SNR Estimation.
- Complete TX and RX chain integration and board testing.
- Functional verification using Questasim for various test cases.

Technologies: Verilog, Questasim, Xilinx Ultrascale FPGA

Senior Staff Engineer - Intel, Malaysia (ORAN 5G NR Specification with Configurable Bandwidth & Multiple Numerology)

Duration: Nov 2022 – May 2025

Summary: Development of ORAN 5G NR IPs including JESD204C/D interfaces and PTP IP integration, targeting Intel Agilex FPGA platforms for 5G wireless communication systems.

Responsibilities:

- RTL design and microarchitecture for JESD204C and JESD204D IPs.
- Board testing with Intel Agilex FPGA.
- Simulation and Signal Tap analysis for various test cases.
- Leading a team of 5 members for timely delivery of RTL modules.

Technologies: Verilog, SystemVerilog, Intel Quartus 23.3, VCS, Verdi, Intel Agilex FPGA

Technical Leader, FPGA - Nokia, Bangalore, India (5G NR Airphone with Configurable Bandwidth & 15 KHz Subcarrier Spacing)

Duration: Nov 2020 – Oct 2022

Summary: Development of 5G NR Airphone physical layer functionalities including PUCCH and PUSCH channel encoding and decoding, implemented on Intel Stratix 10 FPGA.



Responsibilities:

- RTL design for PUCCH F3 and PUSCH modules including CRC, LDPC, and LowPhy.
- Board testing and simulation using Questasim.
- SignalTap analysis for field testing issues.

Technologies: Verilog, VHDL, SystemVerilog, Intel Quartus 19.1, Questasim 2019.3, Intel Stratix 10 FPGA

Lead Engineer - Radisys, Bangalore, India (5G NR OFG-D Base Station Project)

Duration: Aug 2019 – Oct 2020

Summary: Development of 5G NR base station FPGA design including ORAN IP, CPRI Mapper/De-Mapper, and PTP IP integration for synchronization, implemented on Zynq Ultrascale+ FPGA.

Responsibilities:

- Microarchitecture design from requirements and schematic.
- CPRI IP integration and wrapper design.
- ORAN IP design and implementation.
- PTP IP integration for 10ms synchronization.
- PS to PL interface logic generation and HDF generation for software.
- Synthesis, timing closure, and board-level interface and functionality testing.

Technologies: Verilog, SystemVerilog, Xilinx Vivado 2018.2, Questasim 2019.3, Zynq Ultrascale+ FPGA

Lead Engineer - Samsung Research Institute, Bangalore, India (5G NR DAS Board)

Duration: Jan 2019 – July 2019

Summary: Development of 5G NR Distributed Antenna System (DAS) board FPGA design including CPRI IP integration and DDR4 interface, supporting 4 cell and 4 layer configurations.

Responsibilities:

- Microarchitecture design from requirements.
- CPRI IP integration and DDR4 interface design.
- Design of CPRI to SBIF lane mapper.
- PS side logic generation and HDF generation for software.
- Timing closure and board-level interface and functionality testing.
- Separation of IQ samples and bandwidth parameters from CPRI frames.

Technologies: Verilog, VHDL, Xilinx Vivado 2018.3, Zynq Ultrascale FPGA

Lead Engineer - Samsung Research Institute, Bangalore, India (5G Beamforming ASIC)

Duration: June 2018 – Dec 2018

Summary:

- Design and implementation of beamforming ASIC for 5G NR operating at 983



- 04 MHz in 12nm technology, interfacing with DFE ASIC via JESD and PCIe

Responsibilities:

- Microarchitecture and RTL design of DFE interface.
- Linting using Spyglass Lint.
- Synthesis using Design Vision.
- Timing closure and implementation of framing and deframing data paths.
- Implementation of diagnostic functions including CRC-5 and PRBS-31 patterns.
- BIST design between ASIC interfaces.
- Verification test cases and simulation using IES and Verdi.

Technologies: Verilog, SystemVerilog, Synopsys Design Compiler, IES, Verdi, Spyglass Lint

Lead Engineer - Samsung Research Institute, Bangalore, India (5G NR Modem Base Station Board)

Duration: June 2017 – March 2018

Summary: Development of uplink receiver baseband processing modules for 5G NR modem base station, including SRIO interface and FFT processing, implemented on multiple FPGAs.

Responsibilities:

- Microarchitecture design and RTL design of uplink receiver baseband processing modules.
- Design of SRIO interface and FFT modules programmable according to 5G NR specifications.
- High-speed interface wrapper design and interface regression testing.

Technologies: Verilog, Xilinx Vivado

Senior FPGA Design Engineer - Mirafra Technologies India Pvt Ltd (Client: Samsung Research Institute, Bangalore, India) (5G Communication Project)

Duration: June 2016 – June 2017

Summary: FPGA design and verification for 5G communication modem modules, including high-speed interfaces such as JESD, AURORA, and LVDS.

Responsibilities:

- Implementation of FPGA modules from requirements to verification.
- Development of full FPGA testbench and functional verification.
- Worked on high-speed interfaces including JESD, AURORA, and LVDS.
- Used non-project mode Vivado flow.

Technologies: Verilog, VHDL, Xilinx Vivado

VLSI Design Engineer - Sattva eTECH India Pvt Ltd, Bangalore, India (CPU Based PRAN Module for Data Acquisition in Nuclear Power Plant System)

Duration: April 2013 – Feb 2016

Summary: Design and verification of FPGA-based CPU PRAN module for data acquisition system in nuclear power plant (NPCIL, Mumbai).



Responsibilities:

- Implementation and verification of FPGA designs using VHDL.
- Worked in a team of 5 FPGA engineers to successfully implement the PRAN project.
- Documentation of implementation and verification processes.
- Handled clock domain crossing techniques, I/O constraints, clock constraints, false path constraints, and timing analysis.
- RTL synthesis and implementation attributes.

Technologies: VHDL

EDUCATION

- **B.Tech – Electronics & Communications**
MIC college of technology (JNTU, Kakinada, AP), 76.11%
May 2008 - May 2012
- **Class 12th**
Sri Chaitanya Jr College, Vijayawada, 92.00%
Apr 2006 – Mar 2008
- **Class X**
St.Xaviers High School, 82.60%
Apr 2005 - Mar 2006

CERTIFICATION

- **Xilinx Certified VLSI Engineer**
Sandeepani School Of VLSI Design, Bangalore
Sep 2012 – Mar 2013