

Hiring software engineer as easy as calling a taxi.

Marek F.

Embedded (C/C++) Software / FPGA Engineer (VHDL)

SUMMARY

- 7+ years of experience as an Embedded Software Engineer with a focus on C/C++ programming, FPGA development, and VHDL;
- Expertise in developing embedded systems, designing and implementing low-level software for hardware interfaces and device drivers;
- Strong background in FPGA design using VHDL and Verilog, with experience in FPGA programming and hardware/software integration;
- Experience with real-time operating systems (RTOS), and communication protocols such as SPI, I2C, UART, and CAN;
- Proficient in C/C++ programming, with strong debugging skills using tools like GDB, JTAG, and Oscilloscopes;
- Worked on hardware/software co-design and FPGA simulation and verification;
- Familiar with Linux and Windows environments, with cross-compilation for embedded platforms;
- Contributed to designing and developing embedded systems for automotive, telecommunications, and consumer electronics sectors.

SKILLS

Main Technical Skills	FPGA, VHDL, Unix (5 yr.), Intel, XILINX
Programming Languages	C (7 yr.), C#, C++, JavaScript, PHP, x86 Assembly
UI Frameworks, Libraries, and Browsers	CSS, HTML
Databases & Management Systems / ORM	Firebase Realtime Database, MySQL
Azure Cloud Services	Azure Logic Apps
Version Control	BitBucket, Gerrit, Git
Third Party Tools / IDEs / SDK / Services	MatLab, PowerPoint
Mail / Network Protocols / Data transfer	TCP
Operating Systems	Unix (5 yr.)

Other Technical Skills	3D Modelling, Altium, ARM, ASM, AUTOSAR, CAN, FreeRTOS, GPIO, I2C, JTAG, J-Unit, Multisim, Octave, Oscilloscope, RTOS, SPI, UART, USB, VxWorks
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WORK EXPERIENCE

Software Engineer, Wireless Charging Systems Prototyping

Duration: August 2023 - February 2025

Summary: Prototyping of the new generation wireless charging systems in the automotive industry.

Responsibilities: Conducted read and analysis of prototype PCB schematics, customer defect analysis, tested solutions, prototyped interrupt monitors for latency, and integrated with various protocols and systems such as ASM, C, and Autosar OS.

Technologies: ASM, C, ASK, and FSK protocols, EPP and MPP protocols, ADC, Autosar OS, Davinci code generator, Tresos, Qi-Library from NXP.

Software Engineer, CPU & FPGA Cellular Network Emulation

Duration: October 2019 - June 2023

Summary: Development of a complex CPU & FPGA system to emulate the behavior of cellular networks.

Responsibilities: Built an x86 HTML interface and test application for cellular network configuration parameters, managed cell parameters storage and processing through PowerPC processor boards, and configured LTE or 5G cells in FPGA, with communication over SRIO and JIRA for issue tracking.

Technologies: C, C++, VHDL, LTE, 5G, PowerPC, FPGA, SRIO, JIRA.

Embedded Systems Engineer, Power Electronic Device Firmware & RTL Design

Duration: August 2019 - October 2019

Summary: Design firmware and RTL for a Power Electronic Device using an AURIX Microcontroller and ARTIX FPGA.

Responsibilities: Integrated LWIP stack drivers, researched UART drivers for logging and communication, investigated Microblaze firmware, and analyzed circuit schematics and PCB layouts.

Technologies: AURIX 32-bit Tri-Core Microcontroller, ARTIX 7 Xilinx FPGA, LWIP stack, ASCLIN UART drivers, Microblaze firmware.

Junior Hardware Engineer, Live Video Hardware Design

Duration: July 2017 - April 2019



Summary: Design computer hardware for live video capture, processing, and streaming using Intel Altera FPGA technology.

Responsibilities: Created FPGA hardware modules, designed QSYS networks for Nios II processing, managed on-chip memory, tested and debugged RTL modules, integrated BSP and Intel HAL drivers, and analyzed booting codes for embedded systems.

Technologies: VHDL, QSYS, Nios II, Modelsim, Signal Tap, Avalon bus, BSP, Intel HAL.

Junior Hardware Engineer, Embedded Graphical Processing System Prototyping

Duration: July 2017 - April 2019

Summary: Prototyping an embedded graphical processing system using Xilinx FPGA technology and Linux firmware.

Responsibilities: Developed a boot sequence for Zynq Ultrascale MPSoC, customized and modified U-Boot source, and developed communication and debugging tools within a Linux environment.

Technologies: Xilinx FPGA, Linux kernel, U-Boot, XEN Hypervisor, UARTLITE driver, Petalinux, Eclipse.

EDUCATION

The University of Sheffield

Electronics and Communication Engineering Master of Engineering

Open Study College

Pure Mathematics A-Level

Central College Nottingham

Electrical and Electronic Engineering Higher National Diploma

